MOTOROLA

MC1489, A

Quad Line Receivers

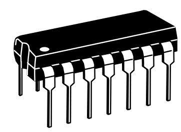
The MC1489 monolithic quad line receivers are designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. EIA–232D.

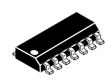
- Input Resistance – 3.0 k to 7.0 kΩ
- Input Signal Range – ± 30 V
- Input Threshold Hysteresis Built In
- Response Control
  - a) Logic Threshold Shifting
  - b) Input Noise Filtering

QUAD MDTL LINE RECEIVERS EIA–232D

SEMICONDUCTOR TECHNICAL DATA

P SUFFIX
PLASTIC PACKAGE
CASE 646



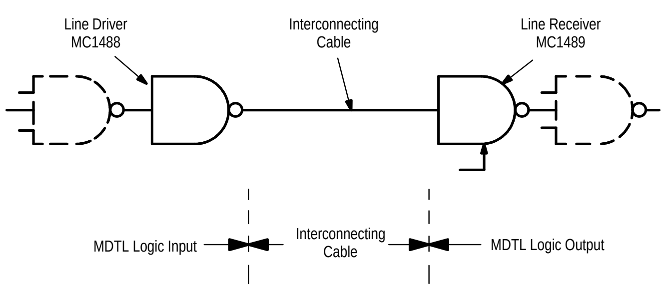


D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

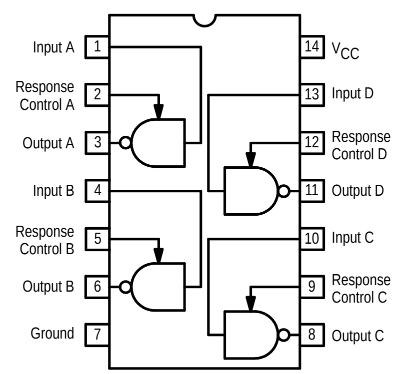
ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC1489P, AP	T_A = 0 to + 75°C	Plastic
MC1489D, AD		SO–14

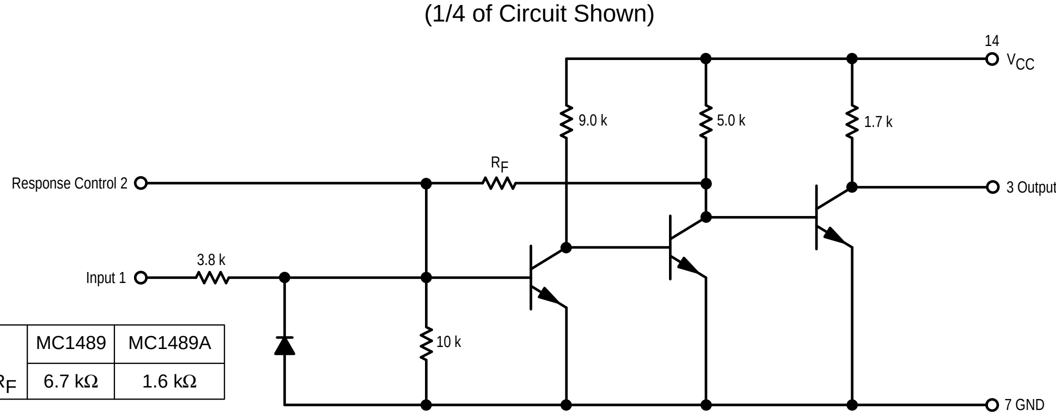
Simplified Application



PIN CONNECTIONS



Representative Schematic Diagram
(1/4 of Circuit Shown)



	MC1489	MC1489A
R_F	6.7 kΩ	1.6 kΩ

MAXIMUM RATINGS (T_A = + 25°C, unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	10	Vdc
Input Voltage Range	V_{IR}	± 30	Vdc
Output Load Current	I_L	20	mA
Power Dissipation (Package Limitation, SO–14 and Plastic Dual In–Line Package) Derate above T_A = + 25°C	P_D $1/\theta_{JA}$	1000 6.7	mW mW/°C
Operating Ambient Temperature Range	T_A	0 to + 75	°C
Storage Temperature Range	T_{stg}	– 65 to + 175	°C

ELECTRICAL CHARACTERISTICS (Response control pin is open.) (V_{CC} = + 5.0 Vdc ± 10%, T_A = 0 to + 75°C, unless otherwise noted)

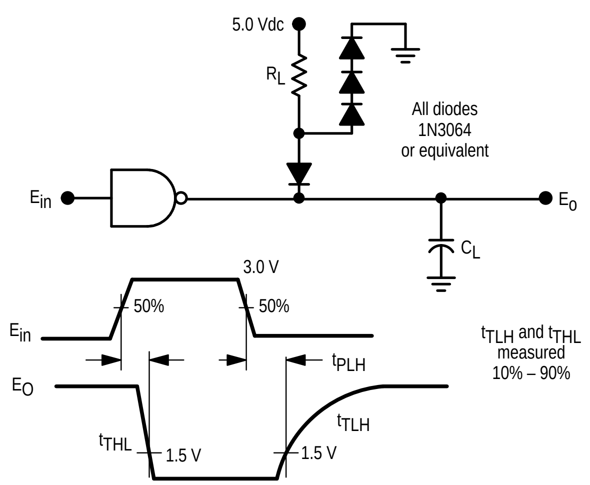
Characteristics		Symbol	Min	Typ	Max	Unit
Positive Input Current	(V_{IH} = + 25 Vdc) (V_{IH} = + 3.0 Vdc)	I_{IH}	3.6 0.43	– –	8.3 –	mA
Negative Input Current	(V_{IH} = – 25 Vdc) (V_{IH} = – 3.0 Vdc)	I_{IL}	– 3.6 – 0.43	– –	– 8.3 –	mA
Input Turn–On Threshold Voltage (T_A = + 25°C, V_{OL} ⩽ 0.45 V)	MC1489 MC1489A	V_{IH}	1.0 1.75	– 1.95	1.5 2.25	Vdc
Input Turn–Off Threshold Voltage (T_A = + 25°C, V_{OH} ⩾ 2.5 V, I_L = – 0.5 mA)	MC1489 MC1489A	V_{IL}	0.75 0.75	– 0.8	1.25 1.25	Vdc
Output Voltage High	(V_{IH} = 0.75 V, I_L = – 0.5 mA) (Input Open Circuit, I_L = – 0.5 mA)	V_{OH}	2.5 2.5	4.0 4.0	5.0 5.0	Vdc
Output Voltage Low	(V_{IL} = 3.0 V, I_L = 10 mA)	V_{OL}	–	0.2	0.45	Vdc
Output Short–Circuit Current		I_{OS}	–	– 3.0	– 4.0	mA
Power Supply Current (All Gates "on," I_{out} = 0 mA, V_{IH} = + 5.0 Vdc)		I_{CC}	–	16	26	mA
Power Consumption	(V_{IH} = + 5.0 Vdc)	P_C	–	80	130	mW

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 Vdc ± 1%, T_A = + 25°C, See Figure 1.)

Characteristics		Symbol	Min	Typ	Max	Unit
Propagation Delay Time	(R_L = 3.9 kΩ)	t_{PLH}	–	25	85	ns
Rise Time	(R_L = 3.9 kΩ)	t_{TLH}	–	120	175	ns
Propagation Delay Time	(R_L = 390 kΩ)	t_{PHL}	–	25	50	ns
Fall Time	(R_L = 390 kΩ)	t_{THL}	–	10	20	ns

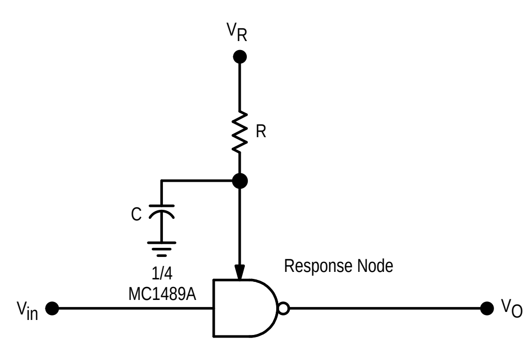
TEST CIRCUITS

Figure 1. Switching Response



C_L = 15 pF = total parasitic capacitance which includes probe and wiring capacitances

Figure 2. Response Control Node



C, capacitor is for noise filtering.
R, resistor is for threshold shifting.

TYPICAL CHARACTERISTICS

(V_{CC} = 5.0 Vdc, T_A = +25°C, unless otherwise noted)

Figure 3. Input Current

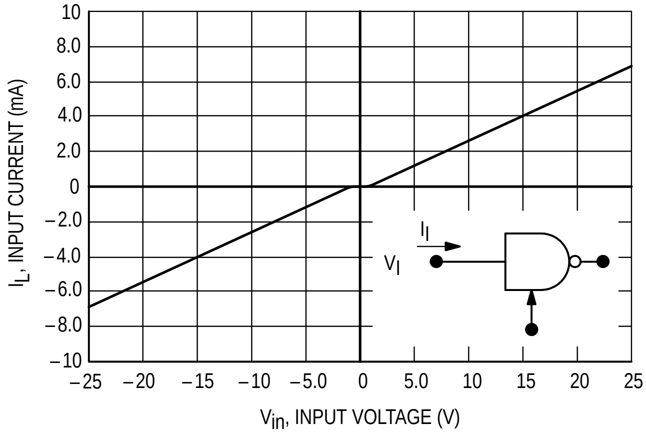


Figure 4. MC1489 Input Threshold Voltage Adjustment

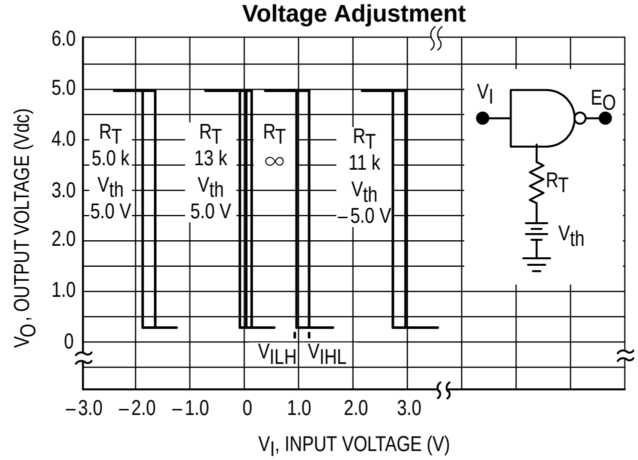


Figure 5. MC1489A Input Threshold Voltage Adjustment

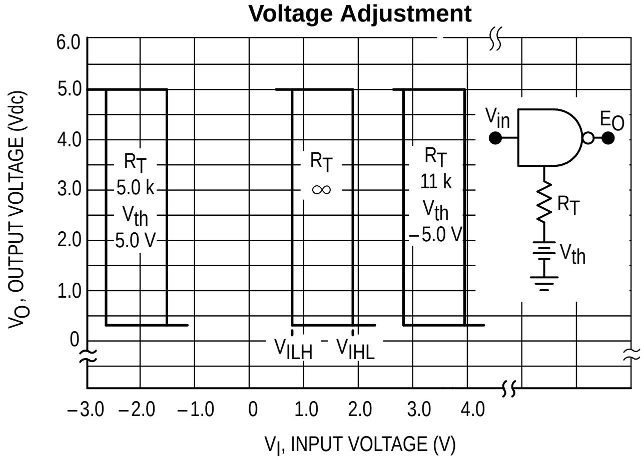


Figure 6. Input Threshold Voltage versus Temperature

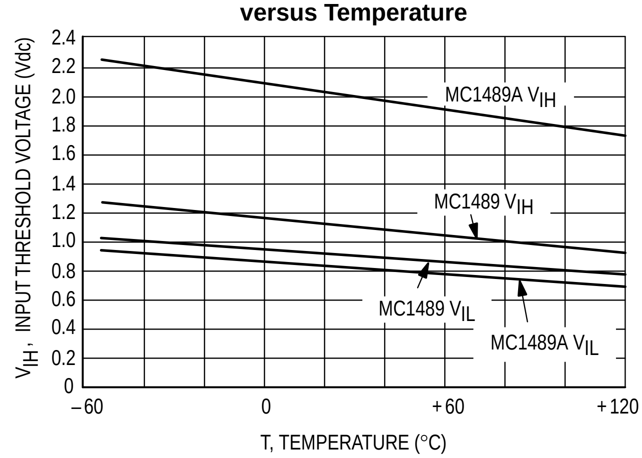
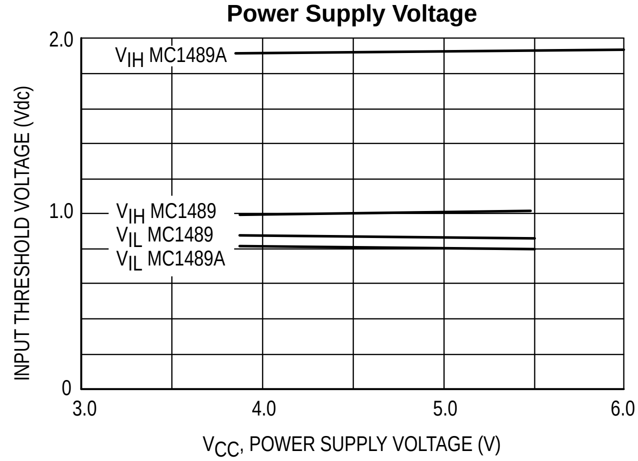


Figure 7. Input Threshold versus Power Supply Voltage



APPLICATIONS INFORMATION

General Information

The Electronic Industries Association (EIA) has released the EIA–232D specification detailing the requirements for the interface between data processing equipment and data communications equipment. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The MC1488 quad driver and its companion circuit, the MC1489 quad receiver, provide a complete interface system between DTL or TTL logic levels and the EIA–232D defined levels. The EIA–232D requirements as applied to receivers are discussed herein.

The required input impedance is defined as between 3000 Ω and 7000 Ω for input voltages between 3.0 and 25 V in magnitude; and any voltage on the receiver input in an open circuit condition must be less than 2.0 V in magnitude. The MC1489 circuits meet these requirements with a maximum open circuit voltage of one V_{BE}.

The receiver shall detect a voltage between – 3.0 and – 25 V as a Logic "1" and inputs between 3.0 and 25 V as a Logic "0." On some interchange leads, an open circuit of power "OFF" condition (300 Ω or more to ground) shall be decoded as an "OFF" condition or Logic "1." For this reason, the input hysteresis thresholds of the MC1489 circuits are all above ground. Thus an open or grounded input will cause the same output as a negative or Logic "1" input.

Device Characteristics

The MC1489 interface receivers have internal feedback from the second stage to the input stage providing input hysteresis for noise rejection. The MC1489 input has typical turn–on voltage of 1.25 V and turn–off of 1.0 V for a typical hysteresis of 250 mV. The MC1489A has typical turn–on of 1.95 V and turn–off of 0.8 V for typically 1.15 V of hysteresis.

Each receiver section has an external response control node in addition to the input and output pins, thereby allowing the designer to vary the input threshold voltage levels. A resistor can be connected between this node and an external power supply. Figures 2, 4 and 5 illustrate the input threshold voltage shift possible through this technique.

This response node can also be used for the filtering of high frequency, high energy noise pulses. Figures 8 and 9 show typical noise pulse rejection for external capacitors of various sizes.

These two operations on the response node can be combined or used individually for many combinations of interfacing applications. The MC1489 circuits are particularly useful for interfacing between MOS circuits and MDTL/MTTL logic systems. In this application, the input threshold voltages are adjusted (with the appropriate supply and resistor values) to fall in the center of the MOS voltage logic levels (see Figure 10).

The response node may also be used as the receiver input as long as the designer realizes that he may not drive this node with a low impedance source to a voltage greater than one diode above ground or less than one diode below ground. This feature is demonstrated in Figure 11 where two receivers are slaved to the same line that must still meet the EIA–232D impedance requirement.

Figure 8. Typical Turn On Threshold versus Capacitance from Response Control Pin to GND

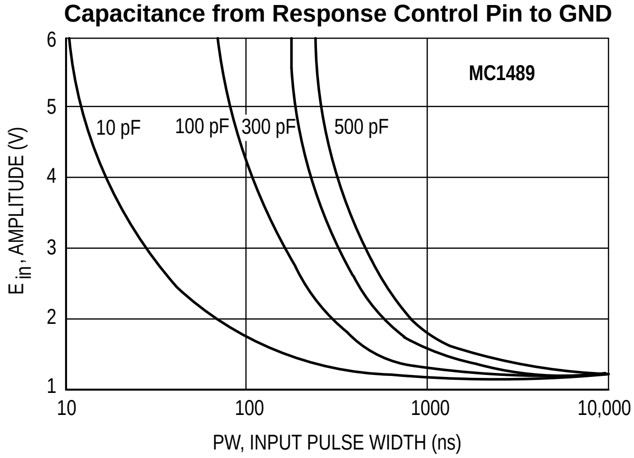


Figure 9. Typical Turn On Threshold versus Capacitance from Response Control Pin to GND

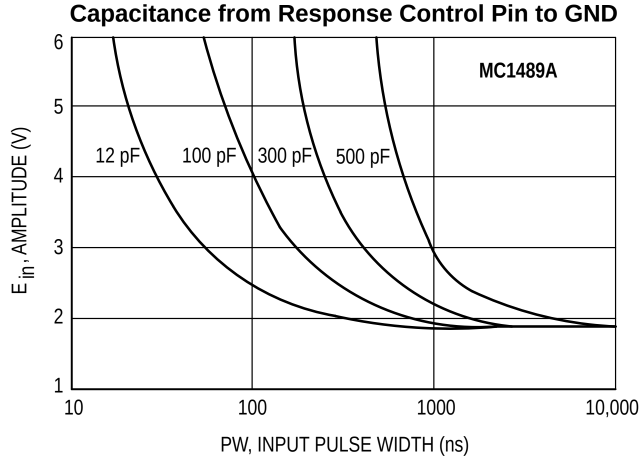


Figure 10. Typical Translator Application – MOS to DTL or TTL

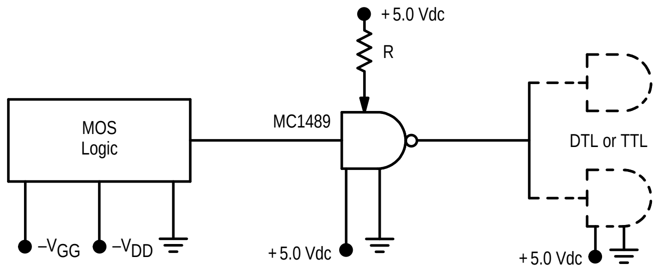
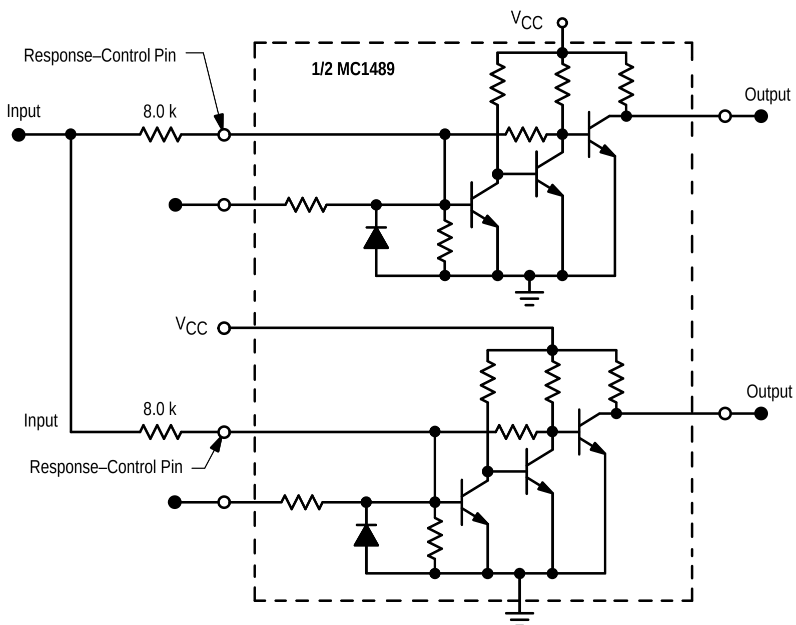
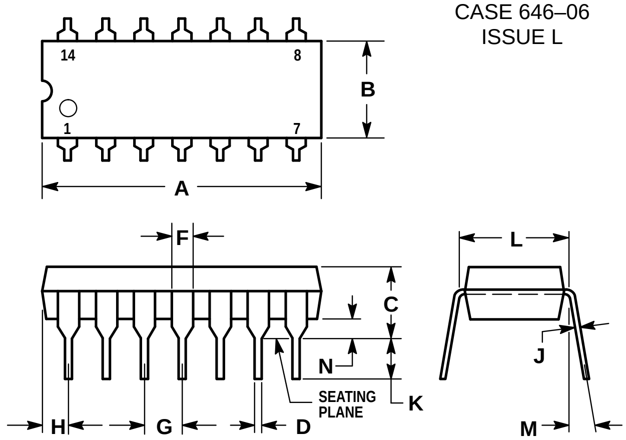


Figure 11. Typical Paralleling of Two MC1489, A Receivers to Meet EIA–232D



OUTLINE DIMENSIONS

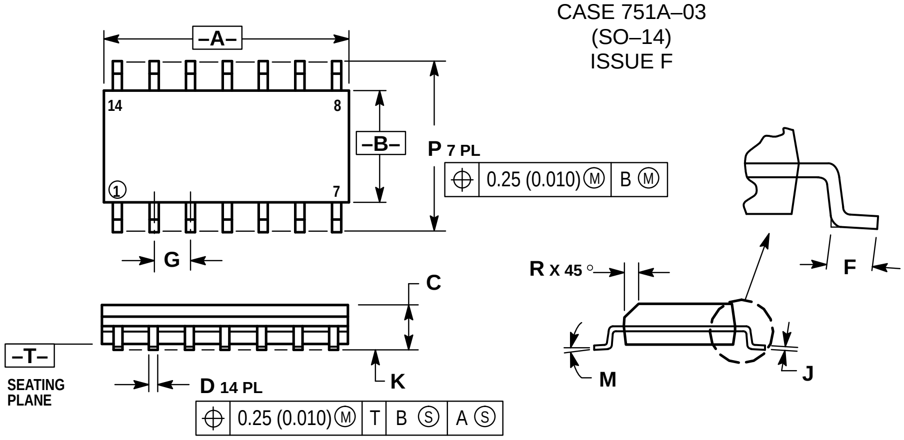
P SUFFIX
PLASTIC PACKAGE
CASE 646–06
ISSUE L



NOTES:
1. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0°	10°	0°	10°
N	0.015	0.039	0.39	1.01

D SUFFIX
PLASTIC PACKAGE
CASE 751A–03
(SO–14)
ISSUE F



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

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